REMARKS

Claims 10-12 are pending in the application. Claim 10 has been amended, leaving claims 10-12 for consideration upon entry of the present amendment. Support for the amendment can be found in Figures 3 and 4C-4E and the corresponding description in the specification (in particular, page 10). Applicant respectfully requests reconsideration in view of the amendment and remarks.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kunii (U.S. 5,412,493) in view of Kawamura (U.S. 5,858,807). For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; and that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

Claims 10-12 include the following limitation: "said second gate insulating film is integrally formed over said first gate insulating film, which covers the semiconductor film, and said second gate insulating film has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode." Kunii and Kawamura do not teach or suggest those limitations.

Kunii shows that the second gate insulating film 8 is present in regions that are not covered with a gate electrode; however, Kunii also shows that the thickness the second gate insulating film 8 does not differ between "a region covered with the gate electrode" and "a region not covered with the gate electrode." The Examiner asserts that Kawamura teaches that limitation. Applicant respectfully traverses.

Kawamura teaches a structure in which a silicon nitride film 8 is formed on a silicon semiconductor layer 7 as a gate insulating film and a gate electrode 11 (Al layer 9 and Mo layer 10) is formed on the gate insulating film. As the Examiner points out, there is a description that a silicon oxide film may be formed on a surface of the silicon semiconductor layer (interface with the silicon nitride film 8 – col. 3, lines 33-37). However, there is no disclosure that the silicon nitride film 8, which is the gate insulating film, has a thickness smaller in a region not covered with the

gate electrode. Instead, in the structure of Kawamura, the "silicon nitride film 8 formed as the gate insulating film" is only present in a region covered with the gate electrode, and thus, it is clear that the thickness of the region not covered with the gate electrode is not taught or suggested.

The Examiner asserts that the silicon nitride insulating film 13 has a smaller film thickness in a region not covered with a gate electrode than a silicon nitride insulating film 8 in a region covered with the gate electrode. Thus, the Examiner asserts that both the silicon nitride insulating film 8 and the silicon nitride insulating film 13 are both the second gate insulating film. Applicant has amended the claim to require that the second gate insulating film is integrally formed over the first gate insulating film. Thus, it is clear that the two films 8 and 13 cannot serve as the second gate insulating film.

Moreover, the two films 8 and 13 cannot serve as the equivalent to the second gate insulating film. The protection layer 13 functions as a protection film by covering the entire element formation region and cannot be integrally formed with the first gate insulating film. It is also clear that the protection layer 13 is formed as a completely different film from the gate insulating film 8.

Moreover, claims 10-12 require that the second gate insulating film, which is integrally formed over the first gate insulating film, has a smaller film thickness in a region not covered with the gate electrode than that in a region covered with the gate electrode. As such, the same second gate insulating film is required to be located both under the gate electrode and in a region that is not under the gate electrode. The claim language requires a comparison of the thickness of the second gate insulating film under the gate electrode to the thickness of the same second gate insulating film in a region not covered with the gate electrode.

Kawamura does not and cannot teach or suggest that limitation. If the Examiner uses the gate insulating film 8 as the equivalent to the second gate insulating film, then that gate insulating film is only located under the gate electrode and has no thickness in a region not covered by the gate electrode. As Figures 1, 2B, and 2C show, the gate insulating film 8 is completely etched away so that it is not located in a region not covered by the gate electrode. Thus, there is no thickness of the gate insulating film 8 in a region not covered with the gate electrode and as such, Kawamura cannot teach or suggest having a smaller film thickness in a region not covered with the

gate electrode than that in a region covered with the gate electrode.

If the Examiner uses the silicon nitride insulating film 13 as the second gate insulating film, then that gate insulating film is only located above the gate electrode and thus, cannot have a thickness under the gate electrode that is different from the thickness of the same second gate insulating film in a region not covered with the gate electrode.

In addition, an Examiner cannot establish obviousness by locating references that describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would have impelled one skilled in the art to do what the patent applicant has done. *Ex parte Levengood*, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. Int. 1993). The references, when viewed by themselves and not in retrospect, must suggest the invention. *In Re Skoll*, 187 U.S.P.Q. 481 (C.C.P.A. 1975). While the Examiner states that the motivation for combining the two references is that Kawamura's teaches would minimize a degradation caused by hot carriers, neither references discusses the advantages of the claimed structure.

In particular, with an integrally formed second gate insulating film, it is possible to reliably prevent intrusion of foreign bodies from the outside into the semiconductor layer. Moreover, because the thickness is smaller than the thickness in a region covered with the gate electrode (although the second gate insulating film is present), it is possible during ion doping to sufficiently and reliably dope an impurity into a semiconductor layer through the second gate insulating film and the first gate insulating film with the gate electrode used as a mask. In addition, the structure of the present invention allows for an effective supply to the semiconductor layer, of hydrogen from the second gate insulating film formed near the semiconductor layer.

In contrast, Kawamura teaches away from such advantage. When the gate insulating film 8 is only present below the gate electrode as described in Kawamura, it is clear that, when ion doping to the semiconductor film or annealing is performed, intrusion of foreign bodies to a region of the semiconductor film not covered with the gate electrode cannot be prevented. None of the references disclose the advantage of preventing intrusion of foreign bodies to the region of the semiconductor film not covered with the gate electrode. Moreover, in Kawamura, the silicon nitride film, which is the gate insulating film, is removed in a region not covered with the gate electrode. Thus, there is no silicon nitride film that blocks ion doping during the doping process to

a portion of the semiconductor layer not covered with the gate electrode.

Specifically, Kawamura teaches an amorphous silicon layer 7a and a silicon nitride film 8 are successively deposited on the insulating substrate 1. On the SiN film 8, gate electrode 11 is formed. With the gate electrode 11 being used as a mask, phosphorus is doped into the amorphous silicon layer 7a, thereby turning a portion of the amorphous silicon layer 7a into an n-type amorphous silicon. Thereafter, the entire surface, including the gate electrode, is covered by a silicon nitride film 13.

The SiN film 13 is clearly different from the second gate insulating film of the present invention. Specifically, in Kawamura, after formation of the gate electrode, ion plantation and laser annealing is applied, and then the SiN film 13 is formed. Claims 10-12 require that the second gate insulating film has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode. Because SiN film 13 is the second insulating film applied in Kawamura and because SiN 13 is not covered with the gate electrode, SiN 13 cannot have a smaller film thickness in a region not covered with the gate electrode than that in a region covered with the gate electrode.

Applicant also respectfully traverses the Examiner's assertion that our argument is not persuasive because it has to do with the process of making the structure. The argument is not about the process of making the claimed structure, but rather the motivation as to why a person skilled in the art would want to combine the references. In this case, because neither references discusses the motivation as to why a person skilled in the art would want to have a second gate insulating film that is integrally formed over said first gate insulating film, and in which the second gate insulating film has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode. The motivation to create such a structure comes from how it is manufactured.

Neither Kunii nor Kawamura provide the motivation to combine the two references to reach the claimed invention. Because SiN film 13 is not formed before the doping process, Kawamura is a completely different structure from Kunii and one skilled in the art would not combine the two references. Kawamura does not recognize the idea of preventing intrusion of impurities into the region of the semiconductor film not covered with the gate electrode.

Accordingly, there is nothing in Kawamura that suggests changing the thickness of the second gate insulating film between the region under the gate electrode and other regions. In addition, the advantages of the arrangement as claimed in claims 10-12 is explained on page 15, lines 18-23. Specifically, having a larger thickness in the gate electrode region allows the ion doping to be blocked at the gate electrode. In addition, having a smaller thickness in a region not covered by the gate electrode does not block the ion doping into the source and drain region and yet prevents intrusion of impurities or the like, thereby improving reliability of the thin film transistor. Accordingly, because there is nothing in Kunii or Kawamura that would motivate one skilled in the art to combine the two references, Applicant respectfully requests that this rejection be withdrawn.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogawa (JP 5-335578) in view of Kawamura. Claims 10-12 include the following limitation: "said second gate insulating film is integrally formed over said first gate insulating film, which covers the semiconductor film, and said second gate insulating film has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode." Ogawa and Kawamura do not teach or suggest those limitations.

Ogawa employs a layered structure of two layers as the gate insulating layer; however, Ogawa does not teach or suggest that the upper gate insulating film on the side of the gate electrode is present in regions that are not covered with the gate electrode. In addition, as explained above, Kawamura does not teach or suggest that limitation. Thus, for the reasons discussed above, claims 10-12 are allowable over Ogawa and Kawamura. Applicant respectfully requests that the rejection be withdrawn.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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April 6, 2004